

low-power ARM-based pax/grsec-enabled server

aka ISO 14001 Cloud - Take 3

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RUMP @ SSTIC2015

Dans l'épisode précédent . . .

NETGEAR ReadyNAS 102

- ▶ SoC Marvell Armada 370 @1.2 GHz (**ARMv7 : Bit NX, FPU**)
- ▶ 512 MB RAM, 128 MB NAND
- ▶ 1 GbE, 2 USB 3.0, 1 USB 2.0, 1 eSATA, 2 ports SATA
- ▶ Console série 3.3v accessible
- ▶ 100 €



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- ▶ Console série 3.3v accessible
- ▶ 100 € [150 € pour le RN104 (4-baies / 2 GbE / LCD)]



Bottom line

Tous les NAS NETGEAR à base d'ARM sont maintenant supportés **mainline**

- ▶ **Duo v2** : 2 DD, ARMv5TE, 256MB RAM, 1 GbE
- ▶ **NV+ v2** : 4 DD, ARMv5TE, 256MB RAM, 1 GbE
- ▶ **RN102** : 2 DD, **ARMv7**, 512MB RAM, 1 GbE, USB 3.0, eSATA
- ▶ **RN104** : 4 DD, **ARMv7**, 512MB RAM, 2 GbE, USB 3.0, eSATA
- ▶ **RN2120** : 4 DD, **1U, 2-core ARMv7**, 2GB, 2GbE, USB 3.0, eSATA



<http://natisbad.org/nas-kernels>

Kernel version 3.17.1-grsec-201410192051

Duo v2 : uImage-3.17.1-grsec-201410192051.duo_v2	[sig] [config] [instructions]
NV+ v2 : uImage-3.17.1-grsec-201410192051.nv+_v2	[sig] [config] [instructions]
RN102 : uImage-3.17.1-grsec-201410192051.rn102	[sig] [config] [instructions]
RN104 : uImage-3.17.1-grsec-201410192051.rn104	[sig] [config] [instructions]
RN2120 : uImage-3.17.1-grsec-201410192051.rn2120	[sig] [config] [instructions]

Kernel version 3.17.1

Duo v2 : uImage-3.17.1.duo_v2	[sig] [config] [instructions]
NV+ v2 : uImage-3.17.1.nv+_v2	[sig] [config] [instructions]
RN102 : uImage-3.17.1.rn102	[sig] [config] [instructions]
RN104 : uImage-3.17.1.rn104	[sig] [config] [instructions]
RN2120 : uImage-3.17.1.rn2120	[sig] [config] [instructions]

Kernel version 3.16.6-grsec-201410092056

Duo v2 : uImage-3.16.6-grsec-201410092056.duo_v2	[sig] [config] [instructions]
NV+ v2 : uImage-3.16.6-grsec-201410092056.nv+_v2	[sig] [config] [instructions]
RN102 : uImage-3.16.6-grsec-201410092056.rn102	[sig] [config] [instructions]
RN104 : uImage-3.16.6-grsec-201410092056.rn104	[sig] [config] [instructions]
RN2120 : uImage-3.16.6-grsec-201410092056.rn2120	[sig] [config] [instructions]

<http://natisbad.org/>

!				MIPv6	m6t	IRO
tips		Duo v2	NV+ v2		RH0	
N810	E4300		RN102	RN104		scapy
	N900	IPv4		RN2120		?

Depuis l'année dernière . . .

Synology DS414 (4 baies, bi-coeur Armada XP @1.33GHz, 380€)



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Synology DS213j (2-bay, single core Armada 370, 190€)



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En cours . . .

Work in progress

Développement en cours d'un support complet pour l'engine crypto du SoC (CESA)

Ce que sait faire le CESA

- ▶ SHA-256, SHA-1, MD5 (et HMAC associés)
- ▶ AES-128, AES-192, AES-256 / modes ECB et CBC
- ▶ Engine DMA

Depuis l'année dernière

- ▶ Travail avec Boris Brezillon (@free-electrons)
- ▶ Soumission en cours

crypto: add a new driver for Marvell's CESA

From: Boris Brezillon <boris.brezillon@free-electrons.com>
To: Herbert Xu <herbert@gondor.apana.org.au>, "David S. Miller" <davem@davemloft.net>, linux-crypto@vger.kernel.org
Subject: [PATCH v3 0/2] crypto: add a new driver for Marvell's CESA
Date: Fri, 22 May 2015 15:33:46 +0200
Message-ID: <1432301642-11470-1-git-send-email-boris.brezillon@free-electrons.com>
Cc: Boris Brezillon <boris.brezillon@free-electrons.com>, Arnaud Ebalard <arno@natisbad.org>, Thomas Petazzoni <thomas.petazzoni@free-electrons.com>, Gregory CLEMENT <gregory.clement@free-electrons.com>, Jason Cooper <jason@lakedaemon.net>, Sebastian Hesselbarth <sebastian.hesselbarth@gmail.com>, Andrew Lunn <andrew@lunn.ch>, Tawfik Bayouk <tawfik@marvell.com>, Lior Amsalem <alior@marvell.com>, Nadav Haklai <nadavh@marvell.com>, Eran Ben-Avi <benavi@marvell.com>, Rob Herring <robh+dt@kernel.org>, Paweł Moll <pawel.moll@arm.com>, Mark Rutland <mark.rutland@arm.com>, Ian Campbell <ijc+devicetree@hellion.org.uk>, Kumar Gala <galak@codeaurora.org>, devicetree@vger.kernel.org

Archive-link: [Article](#), [Thread](#)

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Cc: Boris Brezillon <boris.brezillon@free-electrons.com>, Arnaud Ebalard <arno@natisbad.org>, Thomas Petazzoni <thomas.petazzoni@free-electrons.com>, Gregory CLEMENT <gregory.clement@free-electrons.com>, Jason Cooper <jason@lakedaemon.net>, Sebastian Hesselbarth <sebastian.hesselbarth@gmail.com>, Andrew Lunn <andrew@lunn.ch>, Tawfik Bayouk <tawfik@marvell.com>, Lior Amsalem <alior@marvell.com>, Nadav Haklai <nadavh@marvell.com>, Eran Ben-Avi <benavi@marvell.com>, Rob Herring <robh+dt@kernel.org>, Pawel Moll <pawel.moll@arm.com>, Mark Rutland <mark.rutland@arm.com>, Ian Campbell <ijc+devicetree@hellion.org.uk>, Kumar Gala <galak@codeaurora.org>, devicetree@vger.kernel.org

Archive-link: Article, Thread

.../devicetree/bindings/crypto/marvell-cesa.txt	46 +
arch/arm/boot/dts/armada-370.dtsi	20 +
arch/arm/boot/dts/armada-xp-gp.dts	4 +-
arch/arm/boot/dts/armada-xp.dtsi	31 +
arch/arm/boot/dts/kirkwood.dtsi	2 +-
drivers/crypto/Kconfig	18 +
drivers/crypto/Makefile	1 +
drivers/crypto/marvell/Makefile	2 +
drivers/crypto/marvell/cesa.c	543 +++++++
drivers/crypto/marvell/cesa.h	804 ++++++++
drivers/crypto/marvell/cipher.c	769 ++++++++
drivers/crypto/marvell/hash.c	1349 ++++++++++++++++++
drivers/crypto/marvell/tdma.c	224 +++
drivers/crypto/mv_cesa.c	13 +-

14 files changed, 3816 insertions(+), 10 deletions(-)
create mode 100644 Documentation/devicetree/bindings/crypto/marvell-cesa.txt
create mode 100644 drivers/crypto/marvell/Makefile
create mode 100644 drivers/crypto/marvell/cesa.c
create mode 100644 drivers/crypto/marvell/cesa.h
create mode 100644 drivers/crypto/marvell/cipher.c
create mode 100644 drivers/crypto/marvell/hash.c
create mode 100644 drivers/crypto/marvell/tdma.c

.../devicetree/bindings/crypto/marvell-cesa.txt	46 +
arch/arm/boot/dts/armada-370.dtsi	20 +
arch/arm/boot/dts/armada-xp-gp.dts	4 +-
arch/arm/boot/dts/armada-xp.dtsi	31 +
arch/arm/boot/dts/kirkwood.dtsi	2 +-
drivers/crypto/Kconfig	18 +
drivers/crypto/Makefile	1 +
drivers/crypto/marvell/Makefile	2 +
drivers/crypto/marvell/cesa.c	543 +++++++
drivers/crypto/marvell/cesa.h	804 ++++++++
drivers/crypto/marvell/cipher.c	769 ++++++++
drivers/crypto/marvell/hash.c	1349 ++++++*****
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create mode 100644 drivers/crypto/marvell/cipher.c
create mode 100644 drivers/crypto/marvell/hash.c
create mode 100644 drivers/crypto/marvell/tdma.c

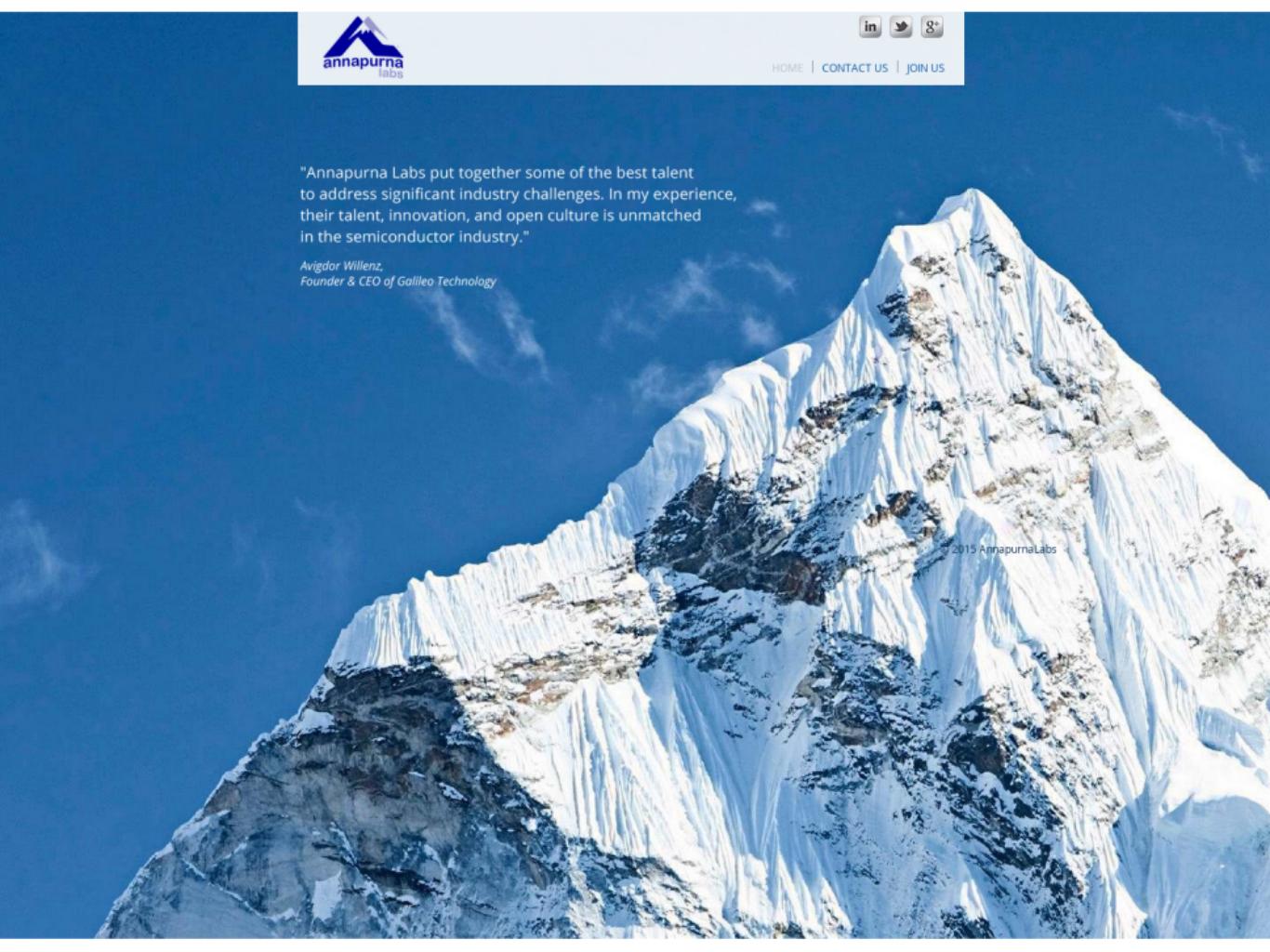
ReadyNAS 204 (4 baies, bi-coeur Cortex A15 AL212 @1.4GHz), 400€



source : <http://www.materiel.net/live/303076.jpg>

"Annapurna Labs put together some of the best talent to address significant industry challenges. In my experience, their talent, innovation, and open culture is unmatched in the semiconductor industry."

*Avigdor Willenz,
Founder & CEO of Galileo Technology*



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Q?