H5TQ2G83DFR

The H5TQ2G83DFR-xxC, H5TQ2G63DFR-xxC, H5TQ2G83DFR-xxI, H5TQ2G63DFR-xxI, H5TQ2G83DFR-xxL, H5TQ2G63DFR-xxL, H5TQ2G83DFR-xxJ, H5TQ2G63DFR-xxJ are a 2,147,483,648-bit CMOS Double Data Rate III (DDR3) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth.

SK Hynix 2Gb DDR3 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock.

While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it.

The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

Features

VDD=VDDQ=1.5V +/- 0.075V
Fully differential clock inputs (CK, /CK) operation
Differential Data Strobe (DQS, /DQS)
On chip DLL align DQ, DQS and /DQS transition with CK transition
DM masks write data-in at the both rising and falling edges of the data strobe
All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
Programmable CAS latency 5, 6, 7, 8, 9, 10, 11, 12, 13 and 14 supported
Programmable additive latency 0, CL-1, and CL-2 supported
Programmable CAS Write latency (CWL) = 5, 6, 7, 8
Programmable burst length 4/8 with both nibble sequential and interleave mode
BL switch on the fly
8banks
Average Refresh Cycle (Tcase of 0 oC~ 95 oC)
- 7.8 µs at 0oC ~ 85 oC
- 3.9 µs at 85oC ~ 95 oC
Commercial Temperature(0oC ~ 85 oC)
Industrial Temperature(-45oC ~ 95 oC)
JEDEC standard 78ball FBGA(x4/x8)
Driver strength selected by EMRS
Dynamic On Die Termination supported
Asynchronous RESET pin supported
ZQ calibration supported
TDQS (Termination Data Strobe) supported (x8 only)
Write Levelization supported
8 bit pre-fetch
This product in compliance with the RoHS directive.

Technical Data Sheet

Part Number	Rev.	Update Date	Remark
H5TQ2G83DFR	1.1	2012-05-16	

Simulation Model

Part Number	Rev.	Update Date	Remark
IBIS	1.01	2012-03-14	H5TQ2G83DFR
IBIS	1.0	2011-10-11	H5TQ2G83DFR-xI
Verilog	1.95	2012-09-25	
HSpice	1.0	2011-10-11	

Ordering Information

Part No.	Configuration	Power Consumption	Temperature	Package
H5TQ2G83DFR-*xxC	256M x 8	Normal Consumption	Commercial	78ball FBGA
H5TQ2G83DFR-*xxI			Industrial	
H5TQ2G83DFR-*xxL		Low Power Consumption (IDD6 Only)	Commercial	
H5TQ2G83DFR-*xxJ			Industrial	
H5TQ2G63DFR-*xxC	128M x 16	Normal Consumption	Commercial	96ball FBGA
H5TQ2G63DFR-*xxI			Industrial	
H5TQ2G63DFR-*xxL		Low Power Consumption (IDD6 Only)	Commercial	
H5TQ2G63DFR-*xxJ			Industrial	

* xx means Speed Bin Grade

OPERATING FREQUENCY

Speed Grade (Marking)	Frequency [Mbps]										Remark (CL-tRCD-tRP)
	CL5	CL6	CL7	CL8	CL9	CL10	CL11	CL12	CL13	CL14	
-G7	667	800	1066	1066							DDR3-1066 7-7-7
-H9	667	800	1066	1066	1333	1333					DDR3-1333 9-9-9
-PB	667	800	1066	1066	1333	1333	1600				DDR3-1600 11-11-11
-RD		800	1066	1066	1333	1333	1600		1866		DDR3-1866 13-13-13
-TE		800	1066	1066	1333	1333	1600		1866	2133	DDR3-2133 14-14-14

* xx means Speed Bin Grade