Computing Memory
Consumer&Network Memory
DDR3 SDRAM
DDR2 SDRAM
DDR SDRAM
SDR SDRAM
Graphics Memory
Mobile Memory
NAND Flash
CMOS Image Sensor
EOL Products
Technical Support

H5TQ1G83DFR

The H5TQ1G6(8)3DFR-xxx series are a 1,073,741,824-bit CMOS Double Data Rate III (DDR3) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. SK Hynix 1Gb DDR3 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

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DDR3 SI
H5TQ1G

Features

DQ Power & Power supply : VDD & VDDQ = 1.5V +/- 0.075V
DQ Ground supply : VSSQ = Ground
Fully differential clock inputs (CK, /CK) operation
Differential Data Strobe (DQS, /DQS)
On chip DLL align DQ, DQS and /DQS transition with CKtransition
DM masks write data-in at the both rising and fallingedges of the data strobe
All addresses and control inputs except data,data strobes and data masks latched on therising edges of the clock
Programmable CAS latency 6, 7, 8, 9, 10, and 11 supported
Programmable additive latency 0, CL-1, and CL-2supported
Programmable CAS Write latency (CWL) = 5, 6, 7, 8
Programmable burst length 4/8 with both nibblesequential and interleave mode
Programmable PASR(Partial Array Self-Refresh) for Digital consumer Applications.
Programmable BL=4 supported (tCCD=2CLK) for Digi-tal consumer Applications.
Programmable ZQ calibration supported

BL switch on the fly

8banks

Average Refresh Cycle (Tcase of 0 °C~ 95 °C)

- 7.8 µs at 0°C ~ 85 °C

- 3.9 µs at 85°C ~ 95 °C

Commercial Temperature (0°C ~ 85 °C)

Industrial Temperature (-40°C ~ 95 °C)

JEDEC standard 78ball FBGA(x8), 96ball FBGA(x16)

Driver strength selected by EMRS

Dynamic On Die Termination supported

Asynchronous RESET pin supported

TDQS (Termination Data Strobe) supported (x8 only)

This product in compliance with the RoHS directive.

Technical Data Sheet

Part Number	Rev.	Update Date	Remark
H5TQ1G83DFR	1.7	2011-09-05	temp. : C, I

Simulation Model

Part Number	Rev.	Update Date	Remark
IBIS	1.4	2010-12-16	H5TQ1G83DFR
IBIS	1.0	2012-07-03	H5TQ1G83DFR-xI
Verilog	1.9	2011-10-31	
HSpice	1.2	2011-10-31	

Ordering Information

Part No.	Configuration	Power consumption	Temperature	Package
H5TQ1G63DFR-*xxC	64M x 16	Normal Consumption	Commercial	96ball FBGA
H5TQ1G63DFR-*xxI		Normal Consumption	Industrial	
H5TQ1G63DFR-*xxL		Low power Consumption (IDD6 Only)	Commercial	
H5TQ1G63DFR-*xxJ		Low power Consumption (IDD6 Only)	Industrial	
H5TQ1G63DFR-*xxP		Low Current consumption	Commercial	
H5TQ1G63DFR-*xxQ		Low Current consumption	Industrial	

* XX means Speed Bin Grade

Part No.	Configuration	Power consumption	Temperature	Package
H5TQ1G83DFR-*xxC	128M x 8	Normal Consumption	Commercial	78ball FBGA
H5TQ1G83DFR-*xxI		Normal Consumption	Industrial	
H5TQ1G83DFR-*xxL		Low power Consumption (IDD6 Only)	Commercial	
H5TQ1G83DFR-*xxJ		Low power Consumption (IDD6 Only)	Industrial	
H5TQ1G83DFR-*xxP		Low Current consumption	Commercial	
H5TQ1G83DFR-*xxQ		Low Current consumption	Industrial	