FDS4435BZ_F085
P-Channel PowerTrench® MOSFET
-30V, -8.8A, 20mΩ

Features
- Max $r_{DS(on)} = 20\, \text{mΩ}$ at $V_{GS} = -10\, \text{V}$, $I_D = -8.8\, \text{A}$
- Max $r_{DS(on)} = 35\, \text{mΩ}$ at $V_{GS} = -4.5\, \text{V}$, $I_D = -6.7\, \text{A}$
- Extended $V_{GS}$ range (-25V) for battery applications
- HBM ESD protection level of ±3.8KV typical (note 3)
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability
- Termination is Lead-free and RoHS compliant
- Qualified to AEC Q101

General Description
This P-Channel MOSFET is produced using Fairchild Semiconductor’s advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Ratings</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>Drain to Source Voltage</td>
<td>-30</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate to Source Voltage</td>
<td>±25</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Drain Current -Continuous $T_A = 25^\circ\text{C}$ (Note 1a)</td>
<td>-8.8</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>-Pulsed</td>
<td>-50</td>
<td></td>
</tr>
<tr>
<td>$P_D$</td>
<td>Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1b)</td>
<td>2.5</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>Power Dissipation $T_A = 25^\circ\text{C}$ (Note 4)</td>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td>$E_{AS}$</td>
<td>Single Pulse Avalanche Energy</td>
<td>24</td>
<td>mJ</td>
</tr>
<tr>
<td>$T_J$, $T_{STG}$</td>
<td>Operating and Storage Junction Temperature Range</td>
<td>-55 to +150</td>
<td>T°C</td>
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</table>

Thermal Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JJC}$</td>
<td>Thermal Resistance, Junction to Case</td>
</tr>
<tr>
<td>$R_{JJA}$</td>
<td>Thermal Resistance, Junction to Ambient (Note 1a)</td>
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Package Marking and Ordering Information

<table>
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<tr>
<th>Device Marking</th>
<th>Device</th>
<th>Package</th>
<th>Reel Size</th>
<th>Tape Width</th>
<th>Quantity</th>
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<tbody>
<tr>
<td>FDS4435BZ</td>
<td>FDS4435BZ_F085</td>
<td>SO-8</td>
<td>13''</td>
<td>12mm</td>
<td>2500 units</td>
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</table>
Electrical Characteristics  \( T_J = 25 ^\circ C \) unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DSS} )</td>
<td>Drain to Source Breakdown Voltage</td>
<td>( I_D = -250 \mu A, V_{GS} = 0V )</td>
<td>-30</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Delta V_{DSS} / \Delta T_J )</td>
<td>Breakdown Voltage Temperature Coefficient</td>
<td>( I_D = -250 \mu A, ) referenced to 25°C</td>
<td>-21</td>
<td>mV/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{DSS} )</td>
<td>Zero Gate Voltage Drain Current</td>
<td>( V_{GS} = -24V, V_{GS} = 0V )</td>
<td>1</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{GSS} )</td>
<td>Gate to Source Leakage Current</td>
<td>( V_{GS} = \pm 25V, V_{DS} = 0V )</td>
<td>±10</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

On Characteristics

\( V_{GS(th)} \)  
Gate to Source Threshold Voltage
\( V_{GS} = V_{DS}, I_D = -250 \mu A \)
-1
-2.1
-3
V

\( \Delta V_{GS(th)} / \Delta T_J \)  
Gate to Source Threshold Voltage Temperature Coefficient
\( I_D = -250 \mu A, \) referenced to 25°C
6
mV/°C

\( r_{D(on)} \)  
Static Drain to Source On Resistance
\( V_{GS} = -10V, I_D = -8.8A \)
16
20
mΩ

\( g_{FS} \)  
Forward Transconductance
\( V_{DS} = -5V, I_D = -8.8A \)
24
S

Dynamic Characteristics

\( C_{iss} \)  
Input Capacitance
\( V_{DS} = -15V, V_{GS} = 0V, f = 1MHz \)
1385
1845
pF

\( C_{oss} \)  
Output Capacitance
\( f = 1MHz \)
275
365
pF

\( C_{rss} \)  
Reverse Transfer Capacitance
230
345
pF

\( R_g \)  
Gate Resistance
\( f = 1MHz \)
4.5
Ω

Switching Characteristics

\( t_{(on)} \)  
Turn-On Delay Time
\( V_{DD} = -15V, I_D = -8.8A, V_{GS} = -10V, R_{GEN} = 6Ω \)
10
20
ns

\( t_r \)  
Rise Time
\( V_{DD} = -15V, I_D = -8.8A, V_{GS} = -10V, R_{GEN} = 6Ω \)
6
12
ns

\( t_{(off)} \)  
Turn-Off Delay Time
30
48
ns

\( t_f \)  
Fall Time
12
22
ns

\( Q_g \)  
Total Gate Charge
\( V_{DD} = 0V \) to -10V
28
40
nC

\( Q_g \)  
Total Gate Charge
\( V_{DD} = 0V \) to -5V
16
23
nC

\( Q_{gs} \)  
Gate to Source Charge
5.2
nC

\( Q_{sd} \)  
Gate to Drain “Miller” Charge
7.4
nC

Drain-Source Diode Characteristics

\( V_{SD} \)  
Source to Drain Diode Forward Voltage
\( V_{DD} = 0V, I_S = -8.8A \)  
(Not 2)
-0.9
-1.2
V

\( t_{rr} \)  
Reverse Recovery Time
\( I_F = -8.8A, di/dt = 100A/\mu s \)
29
44
ns

\( Q_{rr} \)  
Reverse Recovery Charge
23
35
nC

NOTES:
1. \( R_{JA} \) is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. \( R_{JC} \) is guaranteed by design while \( R_{CA} \) is determined by the user’s board design.
2. Pulse Test: Pulse Width < 30μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
4. Starting \( T_J = 25 ^\circ C, L = 1mH, I_{AS} = -7A, V_{DD} = -30V, V_{GS} = -10V \)

\( a. 50 ^\circ C/W \) when mounted on a 1 in² pad of 2 oz copper.

\( b. 125 ^\circ C/W \) when mounted on a minimum pad of 2 oz copper.
Typical Characteristics $T_J = 25^\circ C$ unless otherwise noted

**Figure 1.** On-Region Characteristics

**Figure 2.** Normalized On-Resistance vs Drain Current and Gate Voltage

**Figure 3.** Normalized On-Resistance vs Junction Temperature

**Figure 4.** On-Resistance vs Gate to Source Voltage

**Figure 5.** Transfer Characteristics

**Figure 6.** Source to Drain Diode Forward Voltage vs Source Current
**Typical Characteristics**  $T_J = 25^\circ C$ unless otherwise noted

**Figure 7. Gate Charge Characteristics**

**Figure 8. Capacitance vs Drain to Source Voltage**

**Figure 9. Unclamped Inductive Switching Capability**

**Figure 10. Gate Leakage Current vs Gate to Source Voltage**

**Figure 11. Maximum Continuous Drain Current vs Ambient Temperature**

**Figure 12. Forward Bias Safe Operating Area**
Typical Characteristics  $T_J = 25^\circ C$ unless otherwise noted

Figure 13. Single Pulse Maximum Power Dissipation

Figure 14. Transient Thermal Response Curve

Notes:
- Duty Factor: $D = \frac{t_1}{t_2}$
- Peak $T_J = P_{DM} \times Z_{th,ij} \times R_{th,JA} + T_A$
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<th>Definition</th>
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