FDS4435BZ

P-Channel PowerTrench® MOSFET

-30V, -8.8A, 20mΩ

Features

- Max $r_{DS(on)} = 20m\Omega$ at $V_{GS} = -10V$, $I_D = -8.8A$
- Max $r_{DS(on)} = 35m\Omega$ at $V_{GS} = -4.5V$, $I_D = -6.7A$
- Extended $V_{GSS}$ range (-25V) for battery applications
- HBM ESD protection level of ±3.8KV typical (note 3)
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability
- Termination is Lead-free and RoHS compliant

General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor’s advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance.

This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

MOSFET Maximum Ratings $T_A = 25°C$ unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Ratings</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>Drain to Source Voltage</td>
<td>-30</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate to Source Voltage</td>
<td>±25</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Drain Current -Continuous</td>
<td>$T_A = 25°C$ (Note 1a)</td>
<td>-8.8</td>
</tr>
<tr>
<td></td>
<td>-Pulsed</td>
<td></td>
<td>-50</td>
</tr>
<tr>
<td>$P_D$</td>
<td>Power Dissipation</td>
<td>$T_A = 25°C$ (Note 1a)</td>
<td>2.5</td>
</tr>
<tr>
<td></td>
<td>Power Dissipation</td>
<td>$T_A = 25°C$ (Note 1b)</td>
<td>1.0</td>
</tr>
<tr>
<td>$E_{AS}$</td>
<td>Single Pulse Avalanche Energy</td>
<td></td>
<td>24</td>
</tr>
<tr>
<td>$T_J, T_{STG}$</td>
<td>Operating and Storage Junction Temperature Range</td>
<td></td>
<td>-55 to +150</td>
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Thermal Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JUC}$</td>
<td>Thermal Resistance, Junction to Case</td>
<td>25</td>
</tr>
<tr>
<td>$R_{JUA}$</td>
<td>Thermal Resistance, Junction to Ambient</td>
<td>(Note 1a)</td>
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Package Marking and Ordering Information

<table>
<thead>
<tr>
<th>Device Marking</th>
<th>Device</th>
<th>Package</th>
<th>Reel Size</th>
<th>Tape Width</th>
<th>Quantity</th>
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<tbody>
<tr>
<td>FDS4435BZ</td>
<td>FDS4435BZ</td>
<td>SO-8</td>
<td>13''</td>
<td>12mm</td>
<td>2500units</td>
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</table>
## Electrical Characteristics \( T_J = 25^\circ C \) unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DSS} )</td>
<td>Drain to Source Breakdown Voltage ( i_D = -250\mu A, V_{GS} = 0V )</td>
<td>(-30)</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( \Delta V_{DSS}/\Delta T_J )</td>
<td>Breakdown Voltage Temperature Coefficient ( i_D = -250\mu A, ) referenced to ( 25^\circ C )</td>
<td>(-21)</td>
<td></td>
<td></td>
<td></td>
<td>mV/°C</td>
</tr>
<tr>
<td>( i_{DS} )</td>
<td>Zero Gate Voltage Drain Current ( V_{DS} = -24V, V_{GS} = 0V )</td>
<td>(1)</td>
<td></td>
<td></td>
<td></td>
<td>(\mu A)</td>
</tr>
<tr>
<td>( i_{GS} )</td>
<td>Gate to Source Leakage Current ( V_{DS} = \pm 28V, V_{DS} = 0V )</td>
<td>(\pm 10)</td>
<td></td>
<td></td>
<td></td>
<td>(\mu A)</td>
</tr>
</tbody>
</table>

### Off Characteristics

- **\( V_{GS(th)} \)**: Gate to Source Threshold Voltage \( V_{GS} = V_{DS}, i_D = -250\mu A \) \(-1\) \(-2.1\) \(-3\) V
- **\( \Delta V_{GS(th)}/\Delta T_J \)**: Gate to Source Threshold Voltage Temperature Coefficient \( i_D = -250\mu A, \) referenced to \( 25^\circ C \) \(6\) mV/°C
- **\( i_{DS(on)} \)**: Static Drain to Source On Resistance \( V_{DS} = -10V, i_D = -8.8A \) \(16\) \(20\) mΩ
- **\( g_{FS} \)**: Forward Transconductance \( V_{DS} = -5V, i_D = -8.8A \) \(24\) S

### Dynamic Characteristics

- **\( C_{iss} \)**: Input Capacitance \( V_{DS} = -15V, V_{GS} = 0V, f = 1MHz \) \(1385\) \(1845\) pF
- **\( C_{oss} \)**: Output Capacitance \( V_{GS} = -10V, R_{GEN} = 6\Omega \) \(276\) \(365\) pF
- **\( C_{rss} \)**: Reverse Transfer Capacitance \( 230\) \(345\) pF
- **\( R_{g} \)**: Gate Resistance \( f = 1MHz \) \(4.5\) Ω

### Switching Characteristics

- **\( t_{on} \)**: Turn-On Delay Time \( V_{DD} = -15V, i_D = -8.8A, V_{GS} = -10V \) \(10\) \(20\) ns
- **\( t_{r} \)**: Rise Time \( V_{DD} = -15V, i_D = -8.8A, V_{GS} = -10V, R_{GEN} = 6\Omega \) \(6\) \(12\) ns
- **\( t_{off} \)**: Turn-Off Delay Time \( V_{DD} = -15V, i_D = -8.8A, V_{GS} = -10V, R_{GEN} = 6\Omega \) \(30\) \(48\) ns
- **\( t_{f} \)**: Fall Time \( V_{DD} = -15V, i_D = -8.8A, V_{GS} = -10V, R_{GEN} = 6\Omega \) \(12\) \(22\) ns
- **\( Q_{g} \)**: Total Gate Charge \( V_{DD} = 0V \) to \(-10V \) \(28\) \(40\) nC
- **\( Q_{gs} \)**: Gate to Source Charge \( V_{DD} = 0V \) to \(-10V \) \(16\) \(23\) nC
- **\( Q_{gd} \)**: Gate to Drain “Miller” Charge \( 5.2\) nC
- **\( Q_{gd} \)**: Gate to Drain “Miller” Charge \( 7.4\) nC

### Drain-Source Diode Characteristics

- **\( V_{SD} \)**: Source to Drain Diode Forward Voltage \( V_{GS} = 0V, i_S = -8.8A \) \(\text{(Note 2)}\) \(-0.9\) \(-1.2\) V
- **\( t_{rr} \)**: Reverse Recovery Time \( i_F = -8.8A, dI/dt = 100A/\mu s \) \(29\) \(44\) ns
- **\( Q_{rr} \)**: Reverse Recovery Charge \( 23\) \(35\) nC

### Notes:

1. \( R_{JA} \) is determined with the device mounted on a \( 1in^2 \) pad 2 oz copper pad on a \( 1.5 x 1.5 \) in. board of FR-4 material. \( R_{JC} \) is guaranteed by design while \( R_{CA} \) is determined by the user's board design.

2. Pulse Test: Pulse Width < 30nus, Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

4. Starting \( T_J = 25^\circ C \), \( L = 1mH, i_{DS} = -7A, V_{DD} = -30V, V_{GS} = -10V \)

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Typical Characteristics  $T_J = 25^\circ C$ unless otherwise noted

Figure 1. On-Region Characteristics

Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

Figure 3. Normalized On-Resistance vs Junction Temperature

Figure 4. On-Resistance vs Gate to Source Voltage

Figure 5. Transfer Characteristics

Figure 6. Source to Drain Diode Forward Voltage vs Source Current
Typical Characteristics  $T_J = 25^\circ C$ unless otherwise noted

Figure 7. Gate Charge Characteristics

Figure 8. Capacitance vs Drain to Source Voltage

Figure 9. Unclamped Inductive Switching Capability

Figure 10. Gate Leakage Current vs Gate to Source Voltage

Figure 11. Maximum Continuous Drain Current vs Ambient Temperature

Figure 12. Forward Bias Safe Operating Area

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**Figure 13. Single Pulse Maximum Power Dissipation**

**Figure 14. Transient Thermal Response Curve**

NOTES:
- DUTY FACTOR: $D = t_1/t_2$
- PEAK $T_J = P_{DM} \times Z_{th,JA} \times R_{th,JA} + T_A$

DUTY CYCLE-DESCENDING ORDER

$P_{PEAK}, PEAK TRANSIENT POWER (W)$

$P_{DM}$

$Z_{th,JA}$

$R_{th,JA}$

$R_{th,JA} = 125 \degree C/W$

$V_{GS} = -10 \text{ V}$
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<th>Definition</th>
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<td>Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.</td>
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